

Please cancel claims 1-5.

1    **IN THE CLAIMS**

2  
3    1. (Cancelled) A meta-addressing architecture for a network of dynamically reprogrammable  
4    processing machines, the meta-address specifying a local memory destination for a data  
5    packet comprising:

6           a plurality of addressing machines, each addressing machine having a unique  
7           geographic address, for servicing interrupts, generating and  
8           transmitting meta-addresses comprising of a geographic address and a  
9           local address, and queuing messages;

10          a plurality of dynamically reprogrammable processing machines (DRPMs),  
11          each dynamically reprogrammable processing machine coupled to at  
12          least one addressing machine, for storing, retrieving, and processing  
13          data from a local memory unit responsive to received local-addresses;

14          a plurality of memory units, each memory unit associated with a DRPM; and  
15          an interconnect unit, coupled to the addressing machines, for routing data  
16          between addressing machines responsive to the geographic address of  
17          the meta-address.

1    2. (Cancelled) The addressing machine of claim 1, wherein at least one of the addressing  
2    machines further comprising:

3           an address decoder, for decoding a received meta-address into a geographic  
4           address and a local address;

5           a control unit, coupled to the DRPM, local memory, and the address decoder,  
6           for retrieving meta-address information from the local memory  
7           responsive to receiving an imperative from the DRPM, assembling a  
8           data packet responsive to the retrieved meta-address, receiving  
9           geographic and local addresses from the address decoder, and  
10          transmitting a data packet to the DRPM responsive to determining a  
11          decoded geographic address matches an associated geographic address.

- 1 3. (Cancelled) The architecture of claim 1 further comprising:  
2 a plurality of architecture description memory units, each one coupled to a  
3 DRPM, for storing a geographic address for the DRPM to which it is  
4 coupled.
- 1 4. (Cancelled) The apparatus of claim 2 wherein the addressing machine further comprises:  
2 an interrupt handler, coupled to the I/O unit, comprising:  
3 a recognition unit, for identifying interrupt requests;  
4 a comparator, for comparing identified interrupt requests to a stored  
5 list of interrupt requests to verify validity of an interrupt  
6 request; and  
7 interrupt logic, for processing a validated interrupt request in  
8 accordance with stored interrupt handling instructions.
- 1 5. (Cancelled) The meta-addressing architecture of claim 1 wherein the meta-address is 80  
2 bits wide, the geographic address is 16 bits wide, and the local address is 64 bits wide.
- 1 6. A method for processing instructions in a parallel processor architecture having local  
2 processing machines coupled to local addressing machines and local memory, and the  
3 addressing machines are identified by unique geographic identifications and are  
4 interconnected through an interconnection unit, comprising the steps of:  
5 receiving a program instruction  
6 determining if the received program instruction requires a remote operation;  
7 responsive to a remote operation being required, storing remote component  
8 information into local memory; and  
9 issuing an imperative to the local addressing machine to initiate the remote  
10 operation.
- 1 7. The method of claim 6 wherein the addressing machine performs the steps of:  
2 receiving an imperative from the local processing machine;

3           retrieving remote component information from the local memory, wherein the  
4           remote component information comprises a local geographic address, a  
5           remote geographic address, and a remote local memory address;  
6           generating a meta-address responsive to the retrieved remote component  
7           information;  
8           generating a data packet responsive to the generated meta-address; and  
9           sending the data packet to the interconnect unit.

1   8.     A method for addressing memory in a parallel computing environment in which local  
2   processing units are coupled to local memory, local addressing machines, and an interconnect  
3   unit, the addressing machine performing the steps of:

4           receiving a data packet;  
5           decoding the data packet into a geographic address and a local address;  
6           comparing the geographic address to an associated geographic address; and  
7           responsive to the geographic address matching the associated geographic  
8           address, transmitting the data packet to the local processor.

1   9.     The method of claim 8 wherein the step of transmitting the data packet to the local  
2   processor further comprises the step of storing the data packet in a queue for processing by  
3   the local processor.

1   10.    The method of claim 8 further comprising the steps of:

2           receiving data from the local processor;  
3           retrieving remote operation data from the local memory responsive to the  
4           received data;  
5           generating a meta-address from the retrieved data;  
6           generating a data packet responsive to the generated meta-address; and  
7           transmitting the data packet to the interconnect unit.

1   11.    The method of claim 10 wherein retrieving remote operation data comprises  
2   retrieving a remote geographic address and a remote local memory address.

1 12. The method of claim 11 further comprising retrieving a source geographic address  
2 from local memory.

1 13. The method of claim 12 in which architecture description memory is coupled to each  
2 processor and stores a geographic address for the local processor to which it is coupled,  
3 further comprising retrieving a source geographic address from architecture description  
4 memory.

1 14. A method for processing instructions in a parallel processor architecture having local  
2 processing machines coupled to local addressing machines and local memory, and the  
3 addressing machines are identified by unique geographic identifications and are  
4 interconnected through an interconnection unit, comprising the steps of:  
5 receiving an imperative from the local processing machine;  
6 retrieving remote component information from the local memory, wherein the  
7 remote component information comprises a local geographic address, a  
8 remote geographic address, and a remote local memory address;  
9 generating a meta-address responsive to the retrieved remote component  
10 information;  
11 generating a data packet responsive to the generated meta-address; and  
12 sending the data packet to the interconnect unit.

1 15. A method for addressing memory in a parallel computing environment in which local  
2 processing units are coupled to local memory, local addressing machines, and an interconnect  
3 unit, the addressing machine performing the steps of:  
4 receiving data from the local processor;  
5 retrieving remote operation data from the local memory responsive to the  
6 received data;  
7 generating a meta-address from the retrieved data;  
8 generating a data packet responsive to the generated meta-address; and  
9 transmitting the data packet to the interconnect unit.